

2811  
PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application No.: 10/089,588

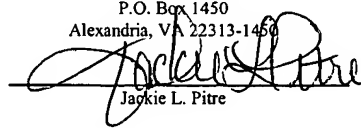
Confirmation No.: 2551

Filing Date: July 15, 2002

Inventors: Bois et al.

Title: SEMICONDUCTOR DEVICE  
COMBINING THE ADVANTAGES  
OF MASSIVE AND SOI  
ARCHITECTURE, AND METHOD  
FOR MAKING SAME

§ Examiner: Unknown  
§ Art Unit: 2811  
§ Atty. Dkt. No.: 5310-04500  
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<b>CERTIFICATE OF MAILING</b> UNDER 37 C.F.R. §1.8
DATE OF DEPOSIT: <u>4/19/05</u>
I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail on the date indicated above and is addressed to: Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450
 Jackie L. Pitre

**INFORMATION DISCLOSURE STATEMENT**

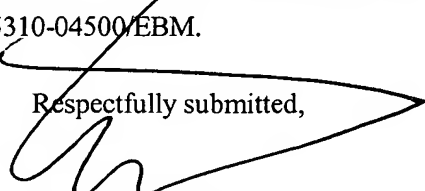
MS: Amendment  
Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

Sir:

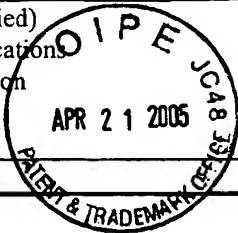
It is respectfully requested that this Information Disclosure Statement be entered and the documents listed on attached Form PTO-1449 (US01-US26, F01-F12, and OA01-OA22) be considered by the Examiner and made of record. Copies of the listed references are enclosed for the convenience of the Examiner.

Should any fees be required, the Commissioner is authorized to charge said fees to Meyertons, Hood, Kivlin, Kowert & Goetzel, P.C. Deposit Account No. 50-1505/5310-04500/EBM.

Respectfully submitted,

  
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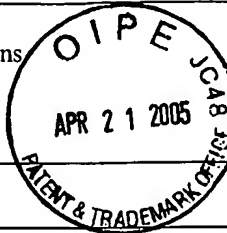
### U.S. PATENT DOCUMENTS

EXAM. INITIALS	REF. DES.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE IF APPROPRIATE
	US01	6475928	11/5/2002	Berenguer et al.			
	US02	6171973	1/9/2001	Schiavone et al.			
	US03	6528341	3/4/2003	Schiavone et al.			
	US04	6215153	4/10/2001	Park			
	US05	5416354	5/16/1995	Blackstone			
	US06	4523213	6/11/1985	Konaka et al.			
	US07	6093592	7/25/2000	Nakabayashi et al.			
	US08	5510645	4/23/1996	Fitch et al.			
	US09	5847439	12/8/1998	Reinberg			
	US10	6064107	5/16/2000	Yeh et al.			
	US11	5595919	1/21/1997	Pan			
	US12	5166765	11/24/1992	Lee et al.			
	US13	4571609	2/18/1986	Hatano			
	US14	5494837	2/27/1996	Subramanian et al.			
	US15	5646058	7/8/1997	Taur et al.			
	US16	5693542	12/2/1997	Suh et al.			
	US17	6037605	3/14/2000	Yoshimura			
	US18	4954871	9/4/1990	Mizutani et al.			
	US19	5834793	11/10/1998	Shibata			
	US20	6091076	7/18/2000	Deleonibus			
	US21	6294812	09/25/01	Ding et al.			
	US22	6667513	12/23/03	Skotnicki et al.			
	US23	6607968	08/19/03	Jurczak et al.			
	US24	6727186	04/27/04	Skotnicki et al.			
	US25	6713356	03/30/04	Skotnicki et al.			
	US26	6150241	11/21/2000	Deleonibus			

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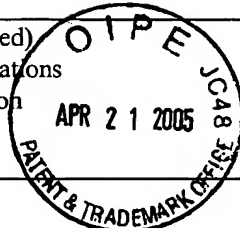
### FOREIGN PATENT DOCUMENTS

EXAM. INITIALS	REF. DES.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	Translation
	F01	10116988	5/6/1998	JP		Abstract
	F02	6120490	4/28/1994	JP		Abstract
	F03	63278375	11/16/1988	JP		Abstract
	F04	11067682	3/9/1999	JP		Abstract
	F05	9723000	6/26/1997	WO		N/A
	F06	19543859	6/27/1996	DE		US5693542
	F07	63266879	11/2/1988	JP		Abstract
	F08	2750534	1/2/1998	FR		US6150241
	F09	05299647	11/12/1993	JP		Abstract
	F10	60175458	9/9/1985	JP		Abstract
	F11	04251939	9/8/1992	JP		Abstract
	F12	04091481	3/24/1992	JP		Abstract

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### OTHER ART

EXAM. INITIALS	REF. DES.	OTHER ART (including Author, Title, Date, Pertinent Pages, etc.)
	OA01	"MOS Transistors with Bottom-Isolated Source/Drain Regions", Research Disclosure, GB, Industrial Opportunities LTD., Havant, no. 398, June 1, 1997, pages 378-379, XP000726504; ISSN: 0374-4353.
	OA02	Rapport De Recherche Europeene for EP 00 40 0672, Date d'achevement de la recherche June 23, 2000 (2 pages)./
	OA03	USPTO Office communication for U.S. Patent Application No. 09/522,794 mailed on July 5, 2001 (8 pages).
	OA04	USPTO Office communication for U.S. Patent Application No. 09/522,794 mailed on March 26, 2002 (8 pages).
	OA05	USPTO Office communication for U.S. Patent Application No. 09/522,794 mailed on September 10, 2002 (4 pages).
	OA06	USPTO Office communication for U.S. Patent Application No. 09/522,794 mailed on December 27, 2002 (9 pages).
	OA07	USPTO Office communication for U.S. Patent Application No. 09/522,794 mailed on July 7, 2003 (9 pages).
	OA08	Rapport d'examen preliminaire international for PCT/FR 00/00641, Date d'achevement du present rapport May 22, 2001 (4 pages).
	OA09	USPTO Office Communication for U.S. Patent Application No. 09/937,056 mailed on July 31, 2002 (9 pages).
	OA10	USPTO Office Communication for U.S. Patent Application No. 09/937,056 mailed on April 10, 2003 (9 pages).
	OA11	Bouillon et al., Ref. XP000753808, "Search for the Optimal Channel Architecture for 0.18/0.12 um Bulk CMOS--Experimental Study", International Electron Devices Meeting 1996, Technical Digest IEDM, San Francisco, December 8, 1996, pages 559-562.
	OA12	International Preliminary Examination Report for PCT/FR00/00642, completed on May 22, 2001 (5 pages).
	OA13	USPTO Office Communication for Application. No. 09/937,108 mailed on April 23, 2002 (9 pages).
	OA14	USPTO Office Communication for Application No. 09/937,108 mailed on April 4, 2003 (3 pages).
	OA15	Rapport de Recherche Internationale for PCT/FR 00/02710 mailed on January 3, 2001 (3 pages).
	OA16	Rapport d'Examen Preliminaire International for PCT/FR00/02710, Date d'achevement du present rapport November 29, 2001 (5 pages).
	OA17	Rapport de Recherche Internationale for PCT/FR 00/00641, Date d'expedition du present rapport de recherché internationale May 11, 2000 (4 pages).
	OA18	International Search Report for PCT/FR 00/2710 mailed on January 3, 2001 (6 pages).
	OA19	U.S. Patent Application No. 09/522,794 filed on March 10, 2000.
	OA20	U.S. Patent Application No. 09/937,056 filed on September 19, 2001.
	OA21	U.S. Patent Application No. 09/937,108 filed on September 19, 2001.
	OA22	Rapport de recherché preliminaire for FR 9903468, Date d'achevement de la recherché December 21, 1999 (2 pages).
	OA23	International Search Report for PCT/FR 00/00642 mailed on July 3, 2000 (6 pages).

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